FIG.1

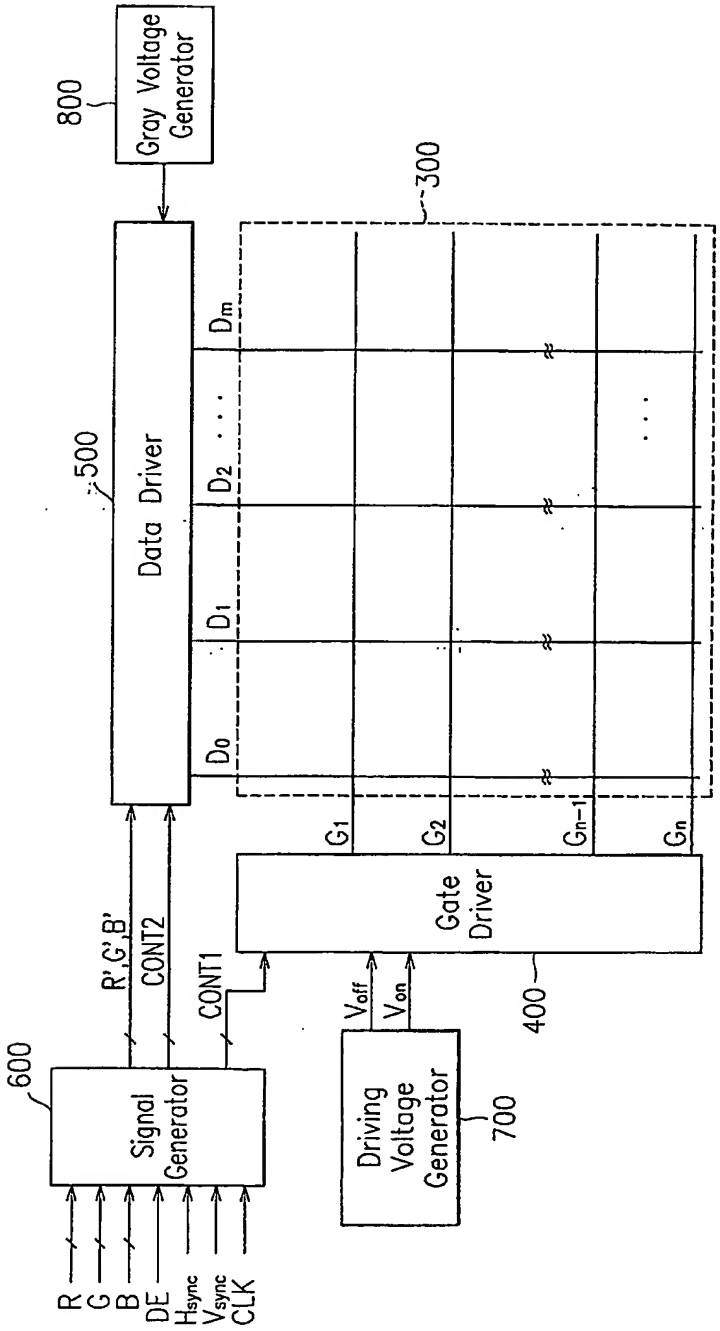

800
Gray Voltage Generator
300
500
Data Driver
D_m
D_2
D_1
D_0
G_1
G_2
G_{n-1}
G_n
Gate Driver
400
R',G',B'
CONT2
CONT1
V_{off}
V_{on}
600
Signal Generator
Driving Voltage Generator
700
R
G
B
DE
H_{sync}
V_{sync}
CLK

FIG.2A

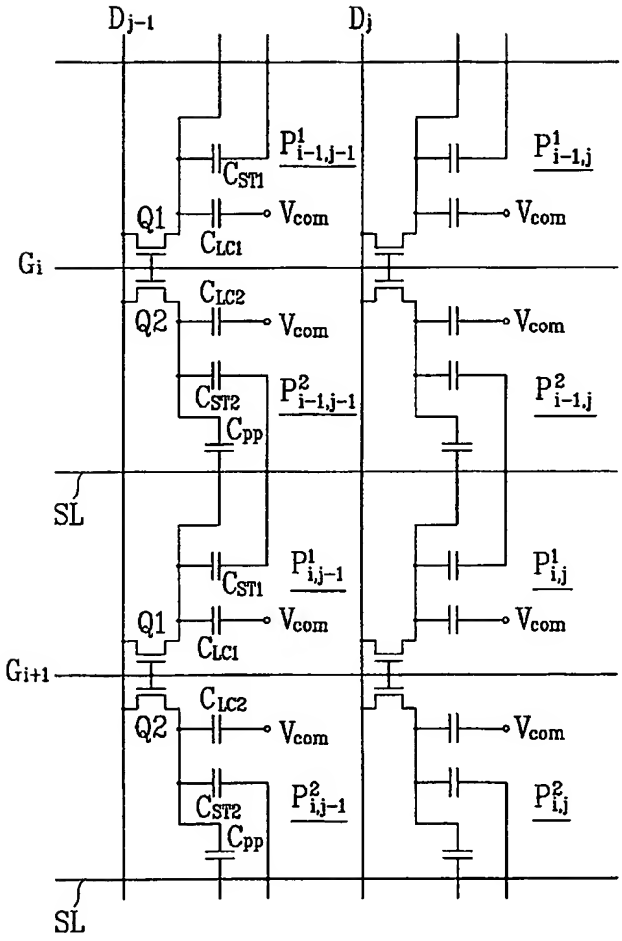

Dj-1
Dj
Gi
Gi+1
SL
SL
Q1
Q2
Vcom
CLC1
CLC2
CST1
CST2
Cpp
P1i-1,j-1
P1i-1,j
P2i-1,j-1
P2i-1,j
P1i,j-1
P1i,j
P2i,j-1
P2i,j

FIG.2B

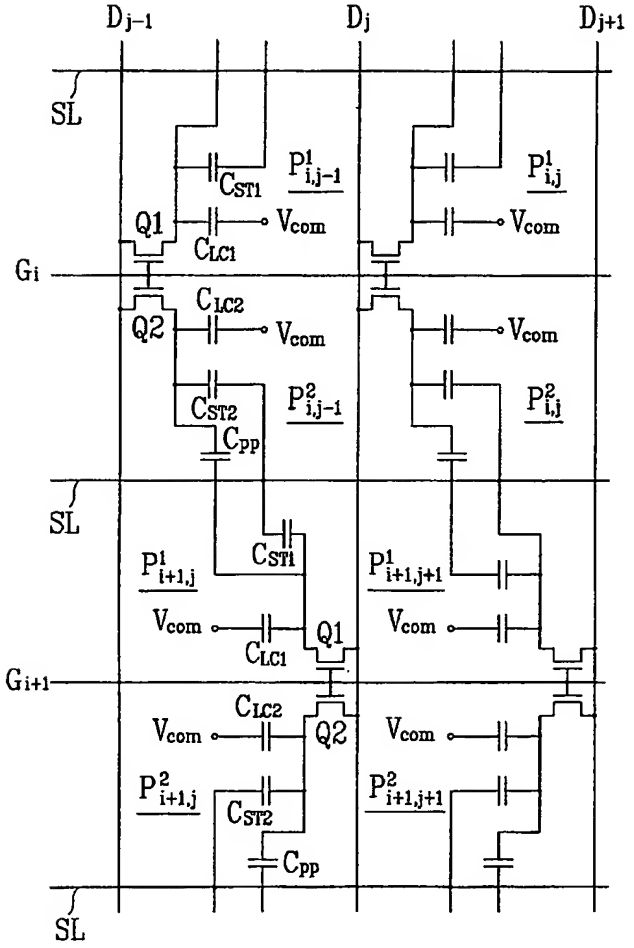

Dj-1
Dj
Dj+1
SL
Gi
Gi+1
Q1
Q2
Vcom
CLC1
CLC2
CST1
CST2
Cpp
P1i,j-1
P1i,j
P2i,j-1
P2i,j
P1i+1,j
P1i+1,j+1
P2i+1,j
P2i+1,j+1

FIG.3

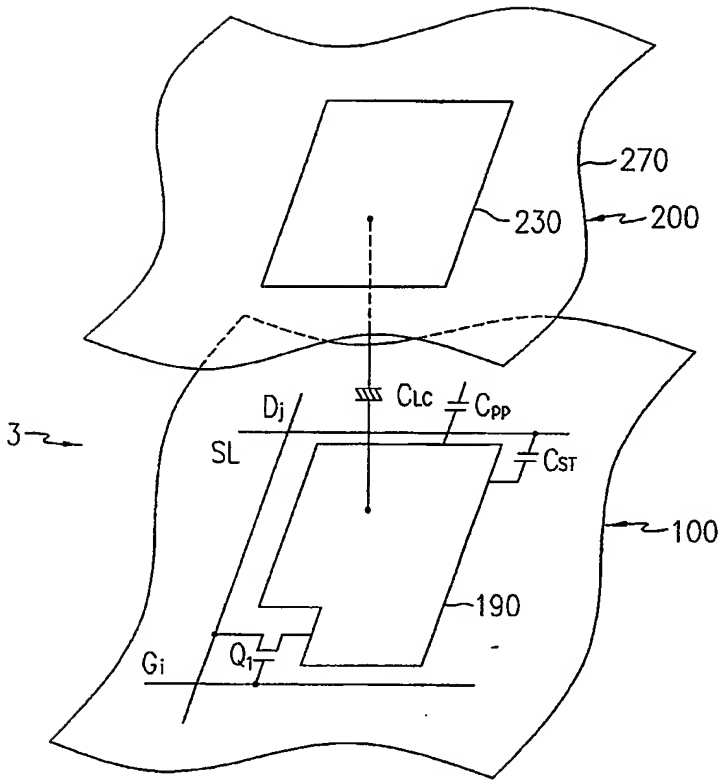


FIG.4

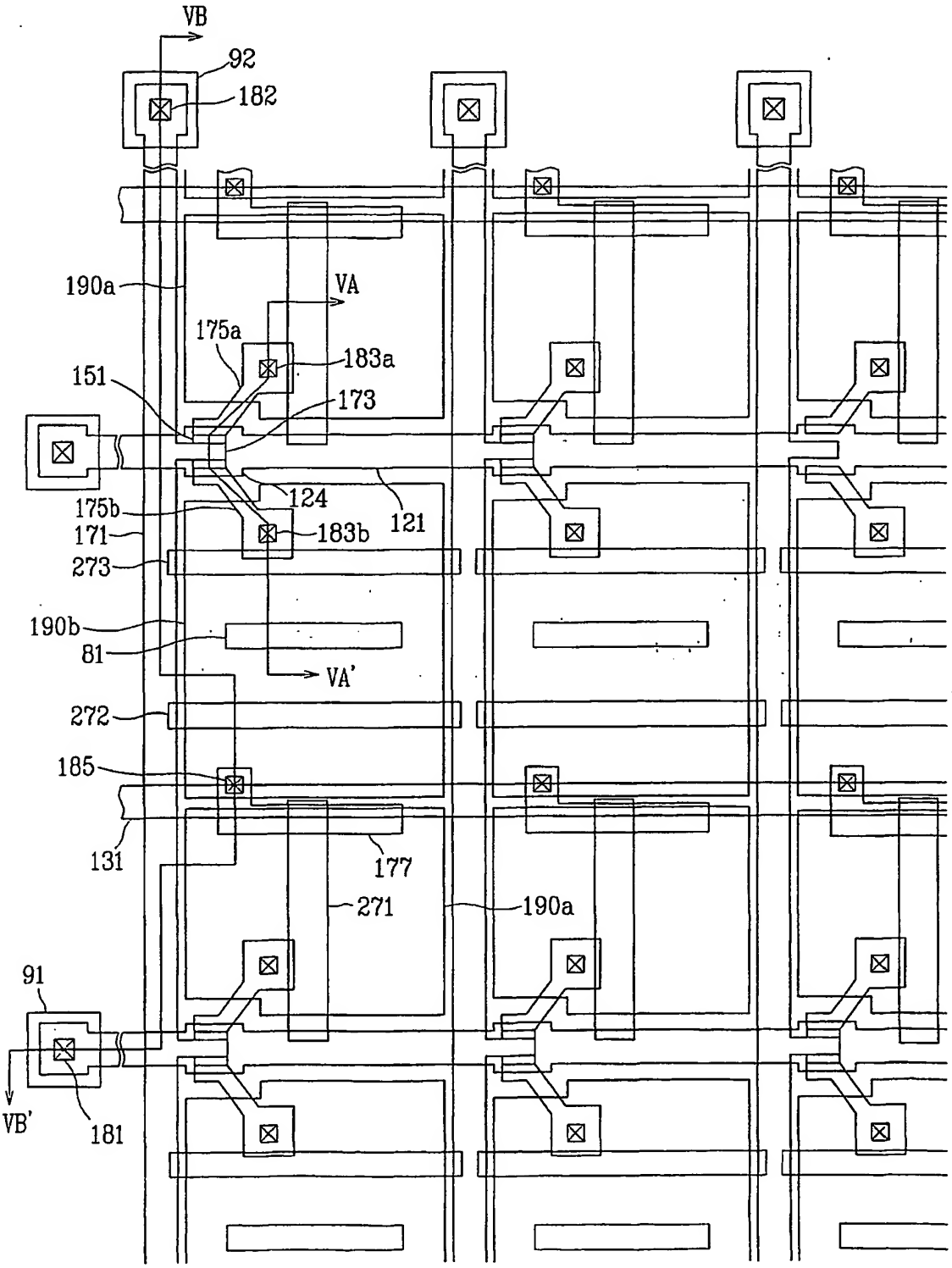

VB
92
182
190a
VA
175a
183a
151
173
124
121
175b
183b
171
273
190b
81
VA'
272
185
131
177
271
190a
91
VB'
181

FIG.5A

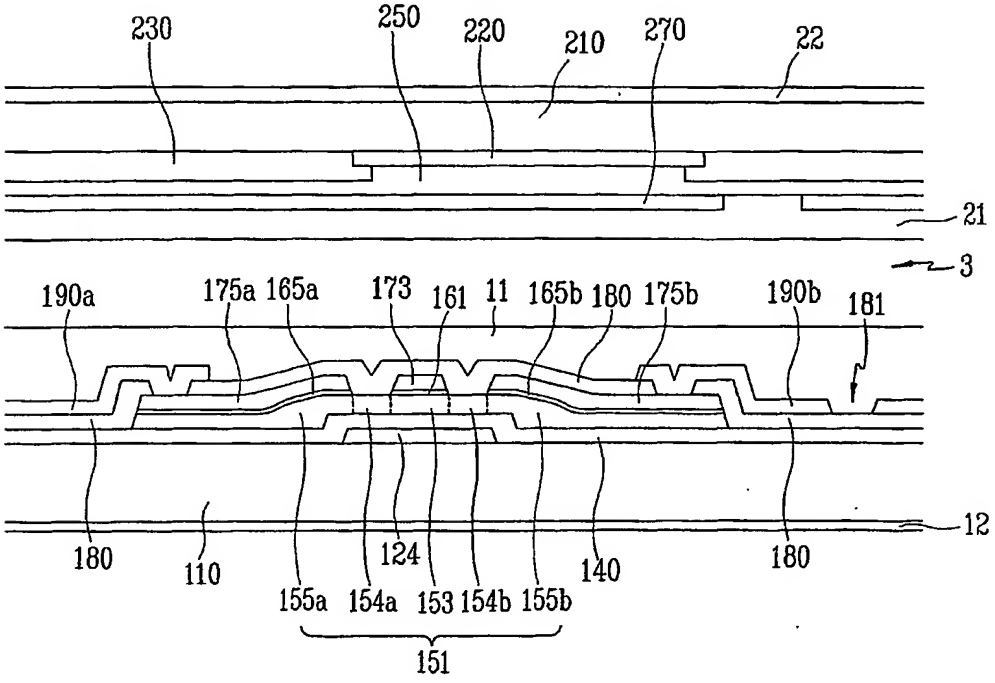

230
250
220
210
270
22
21
3
190a
175a
165a
173
161
11
165b
180
175b
190b
181
12
180
110
124
140
180
155a
154a
153
154b
155b
151

FIG.5B

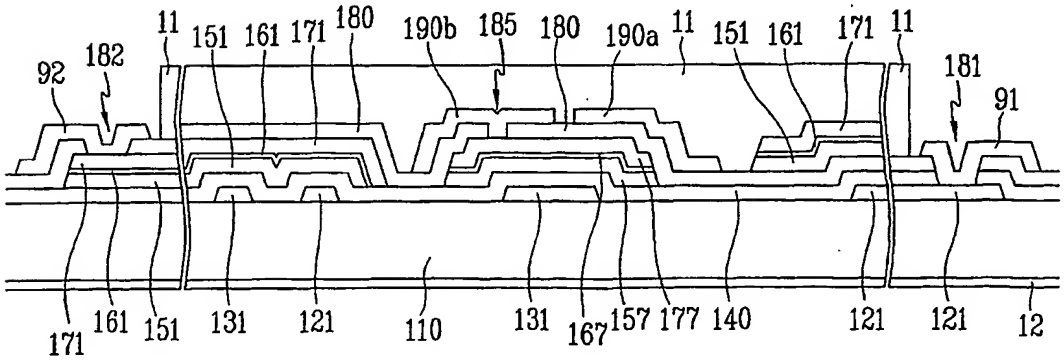

92
182
11
151
161
171
180
190b
185
180
190a
11
151
161
171
11
181
91
171
161
151
131
121
110
131
167
157
177
140
121
121
12

FIG.6

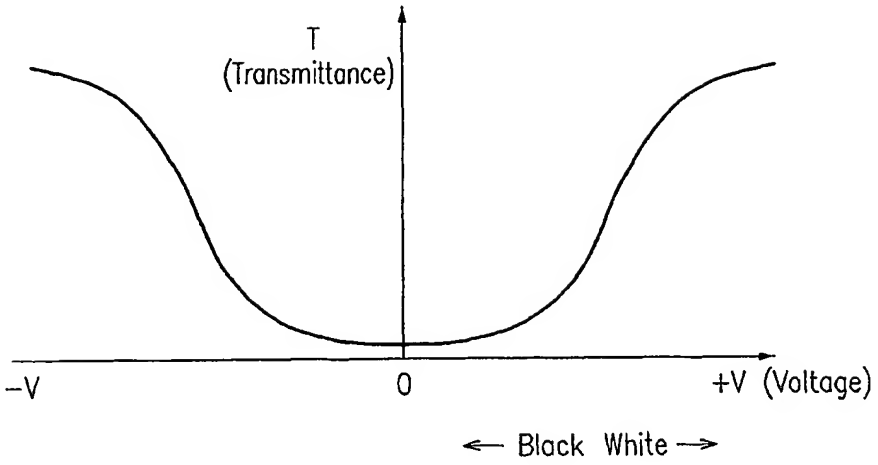

T
(Transmittance)
-V
0
+V (Voltage)
← Black White →

FIG.7

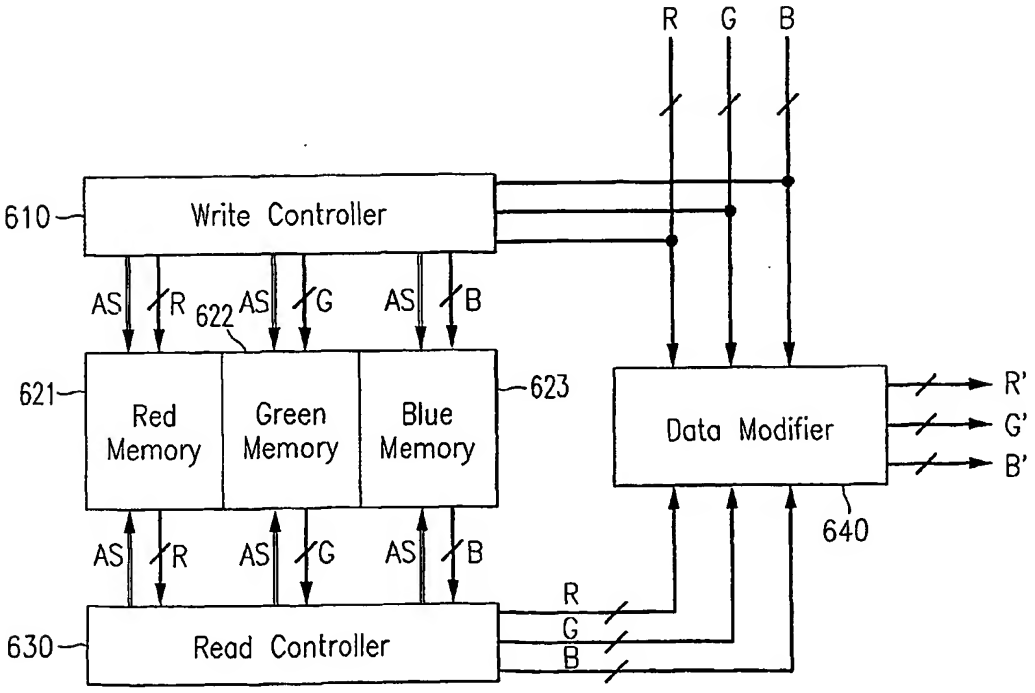
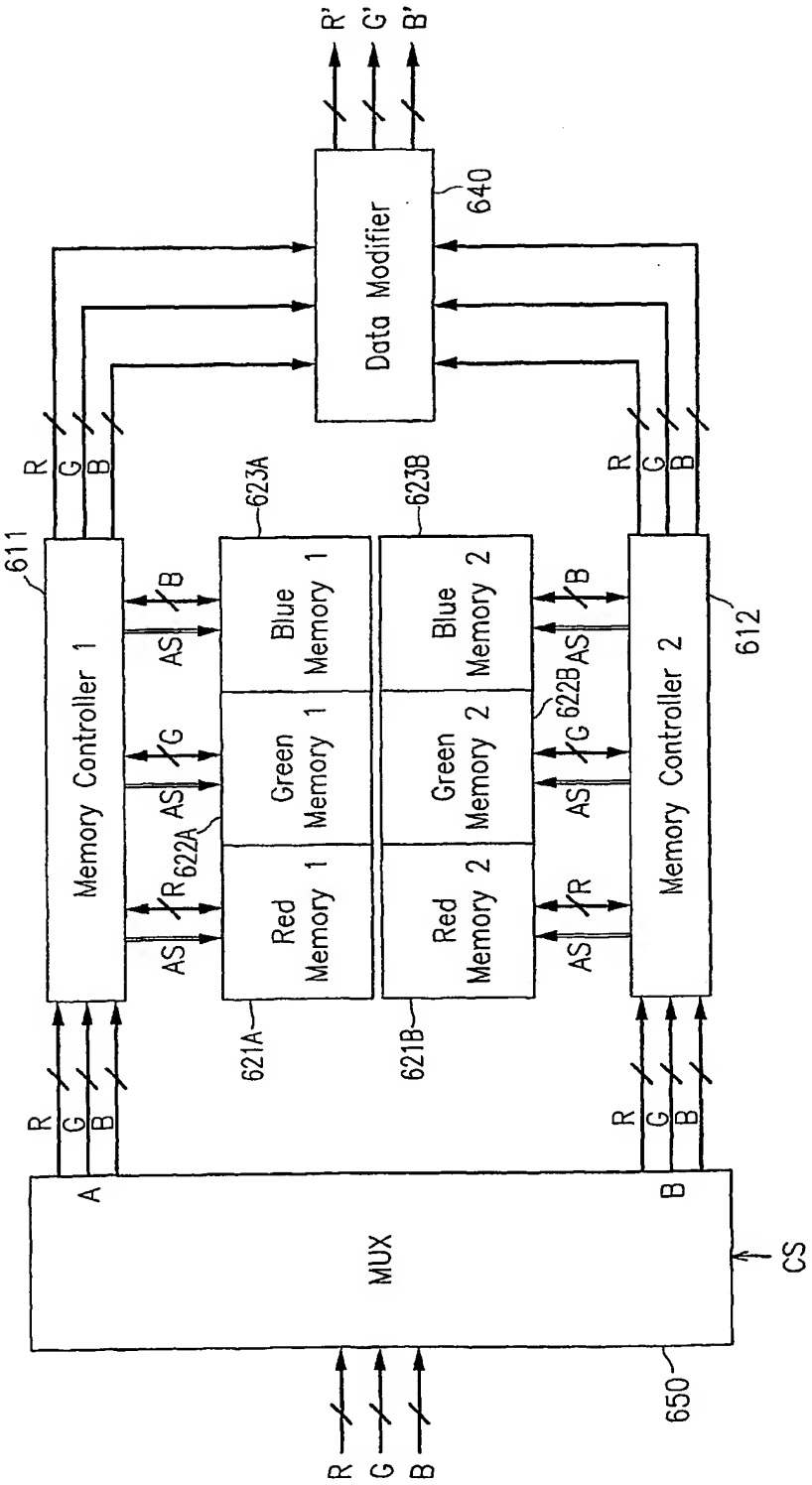

R
G
B
610
Write Controller
AS
R
622
AS
G
AS
B
621
Red Memory
Green Memory
Blue Memory
623
Data Modifier
R'
G'
B'
640
630
Read Controller

FIG.8

Previous \ Current	1	2	. . .	K−1	K
1	1	$X_{2,1}$		$X_{1,K-1}$	$X_{1,K}$
2	$X_{2,1}$	2		$X_{2,K-1}$	$X_{2,K}$
⋮	⋮	⋮	⋮	⋮	⋮
R−1	$X_{R-1,1}$	$X_{R-1,2}$		R−1	$X_{R-1,K}$
R	$X_{R,1}$	$X_{R,2}$		$X_{R,K-1}$	R

FIG.9


R'
G'
B'
Data Modifier
640
R
G
B
611
623A
623B
612
Memory Controller 1
Blue Memory 1
Green Memory 1
Red Memory 1
Blue Memory 2
Green Memory 2
Red Memory 2
Memory Controller 2
AS
622A
622B
621A
621B
A
B
MUX
CS
650